

Hardware Demonstration of the Feasibility and Value of Distributed Resources as a Solution to the Sensitive Load Problem

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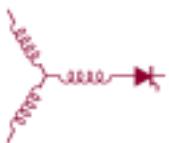
University of Wisconsin-Madison

Holly Thomas

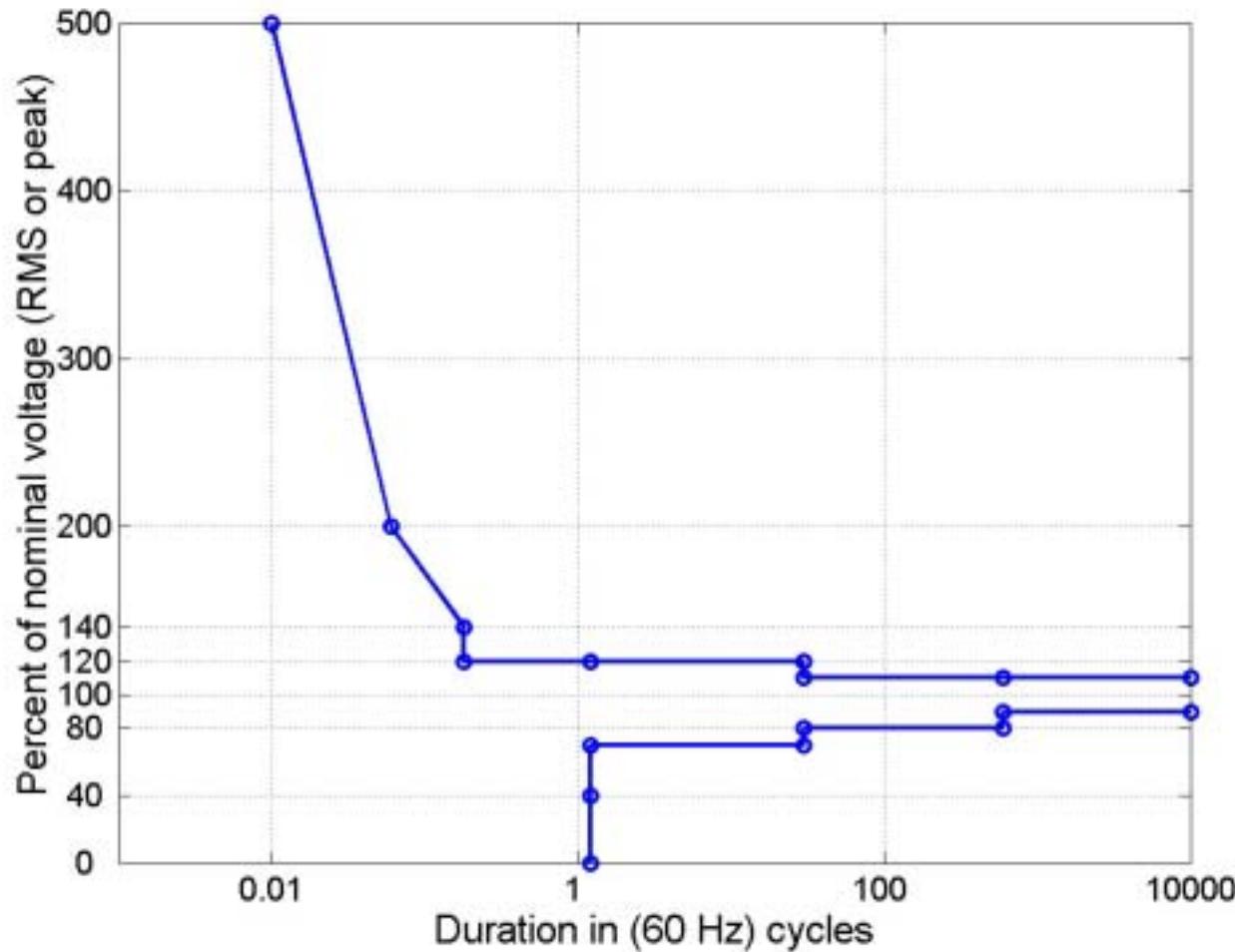
NREL, Technical Monitor

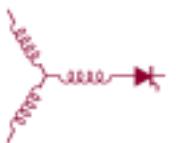
Project Objective

- Enable inverter based DR sources to meet demands of sensitive loads
- Enable parallel clusters of DR sources to operate in a stable manner without communication



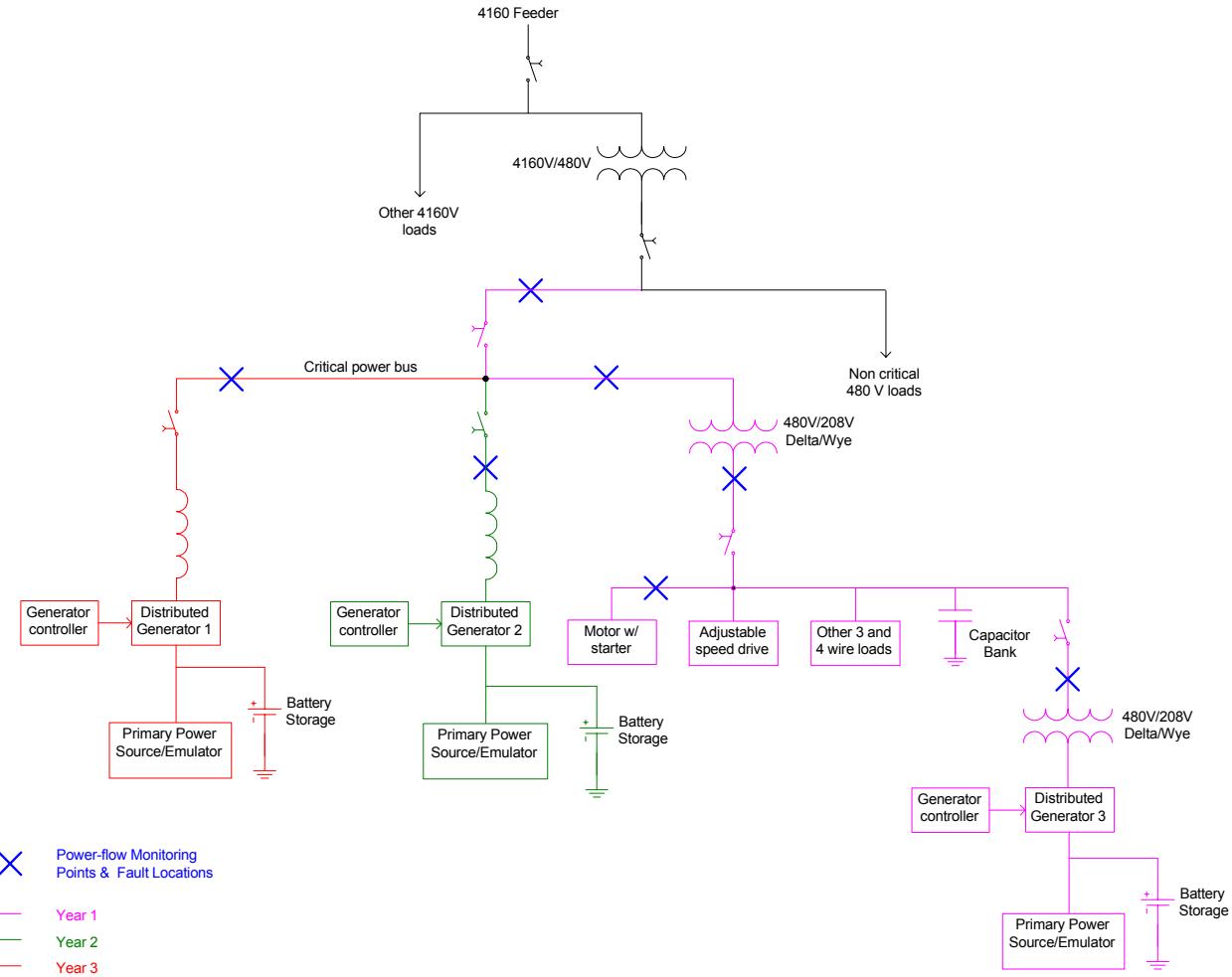
Typical susceptibility limits

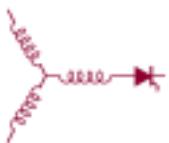




Proposed Hardware Platform

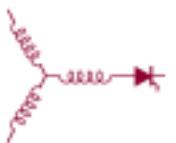
- Three inverters
- 3 wire and 4 wire
- Islanding and reconnection
- Direct & transformer coupling
- Complex loads
- Power source emulation
- Energy storage emulation
- Decentralized control





Control Objectives

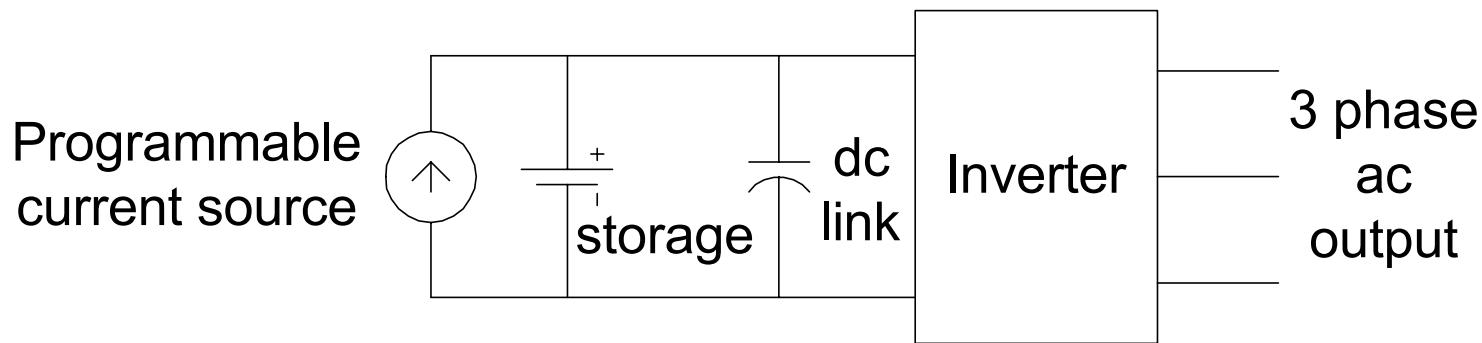
1. Real Power-Frequency Droop Characteristics
2. Reactive Power-Voltage Droop Characteristics
3. Address short term power quality issues
4. Ride through nominal amount of voltage sags and frequency deviations in a benign manner
5. Island and feed local critical loads upon large deviation
6. Reconnect upon system recovery seamlessly



Year 1 Tasks

1. Development of Power Source Emulator (PSE)
2. Study of Energy Storage Requirements (ESR)
3. Demonstration of Operation of Single Inverter (DSI)
4. Development of Inverter with Distributed Generation Control Interface (DGC)
5. Computer Simulation Support (CSS)

Hardware Approach

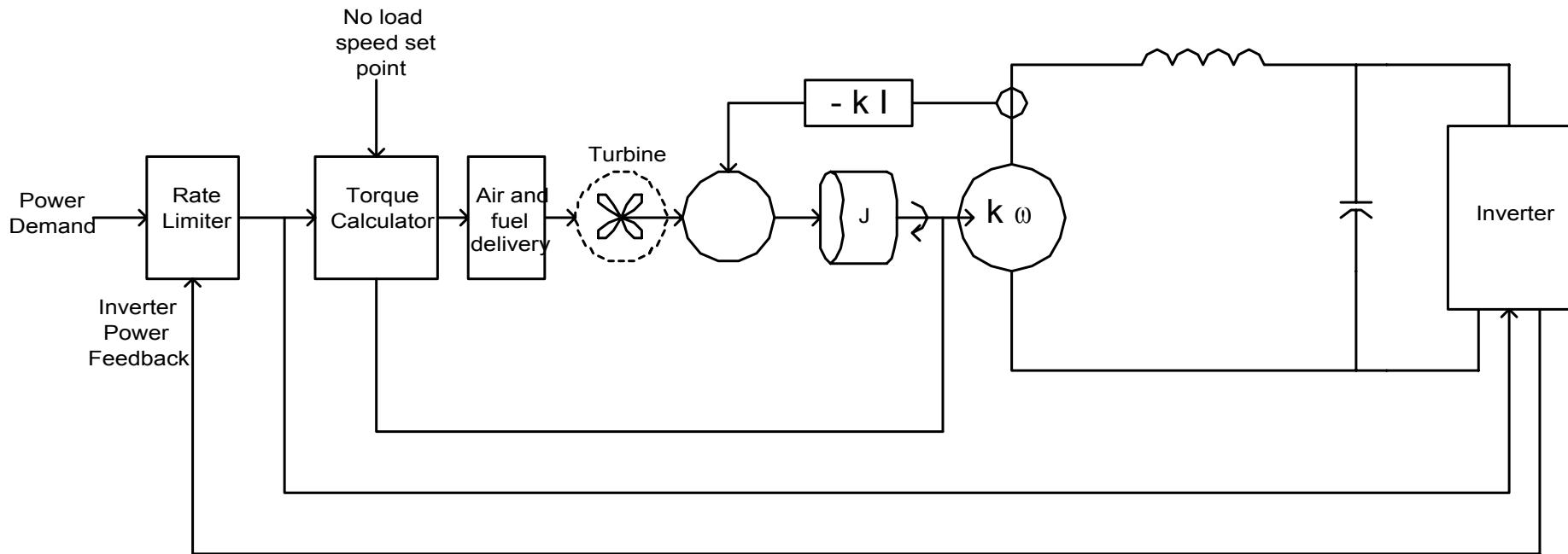


1. PSE

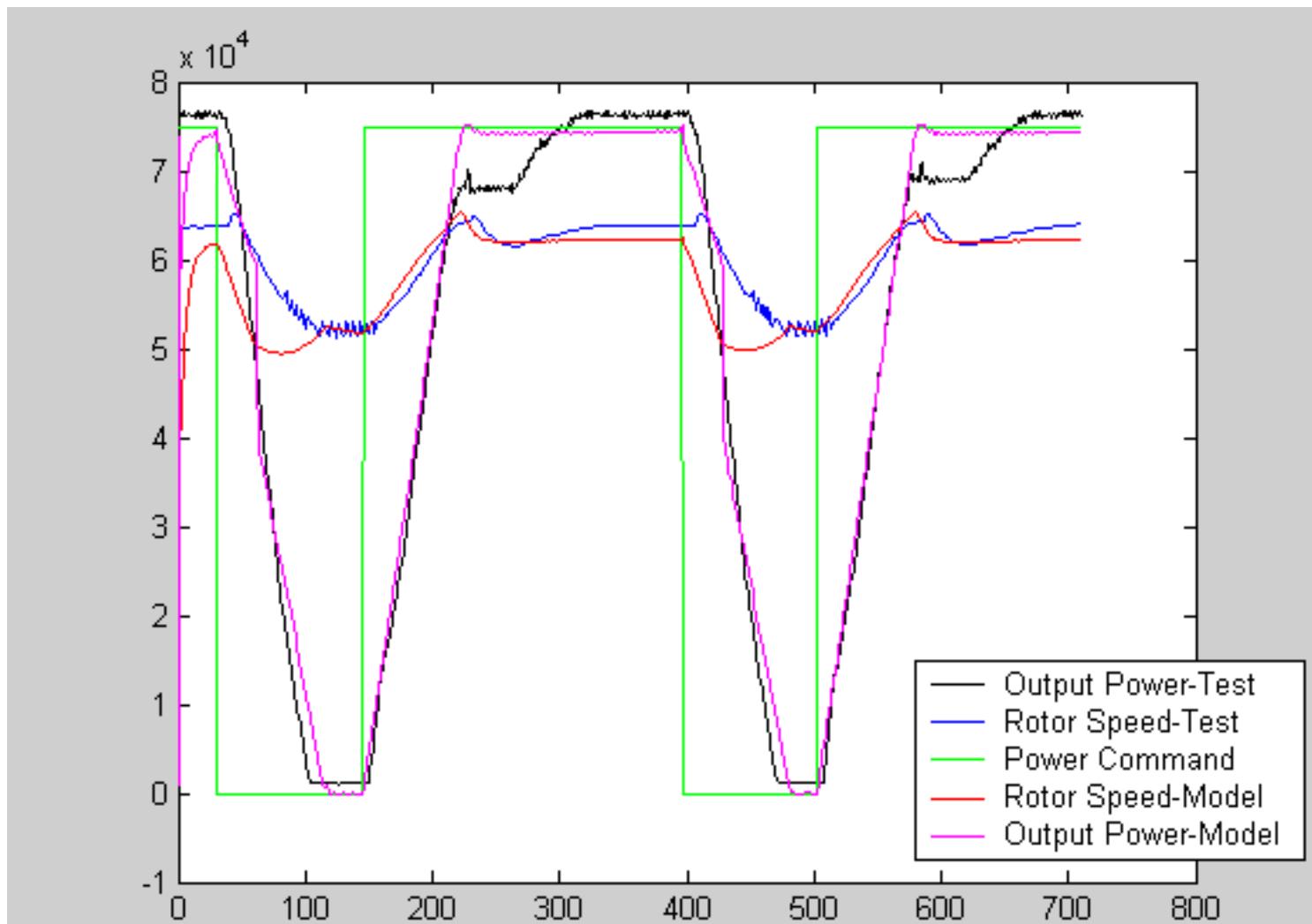


- Programmable voltage and current capability
- Allow source and battery modeling
- Incorporate effects of battery management functions
- Plan B – commercial converter

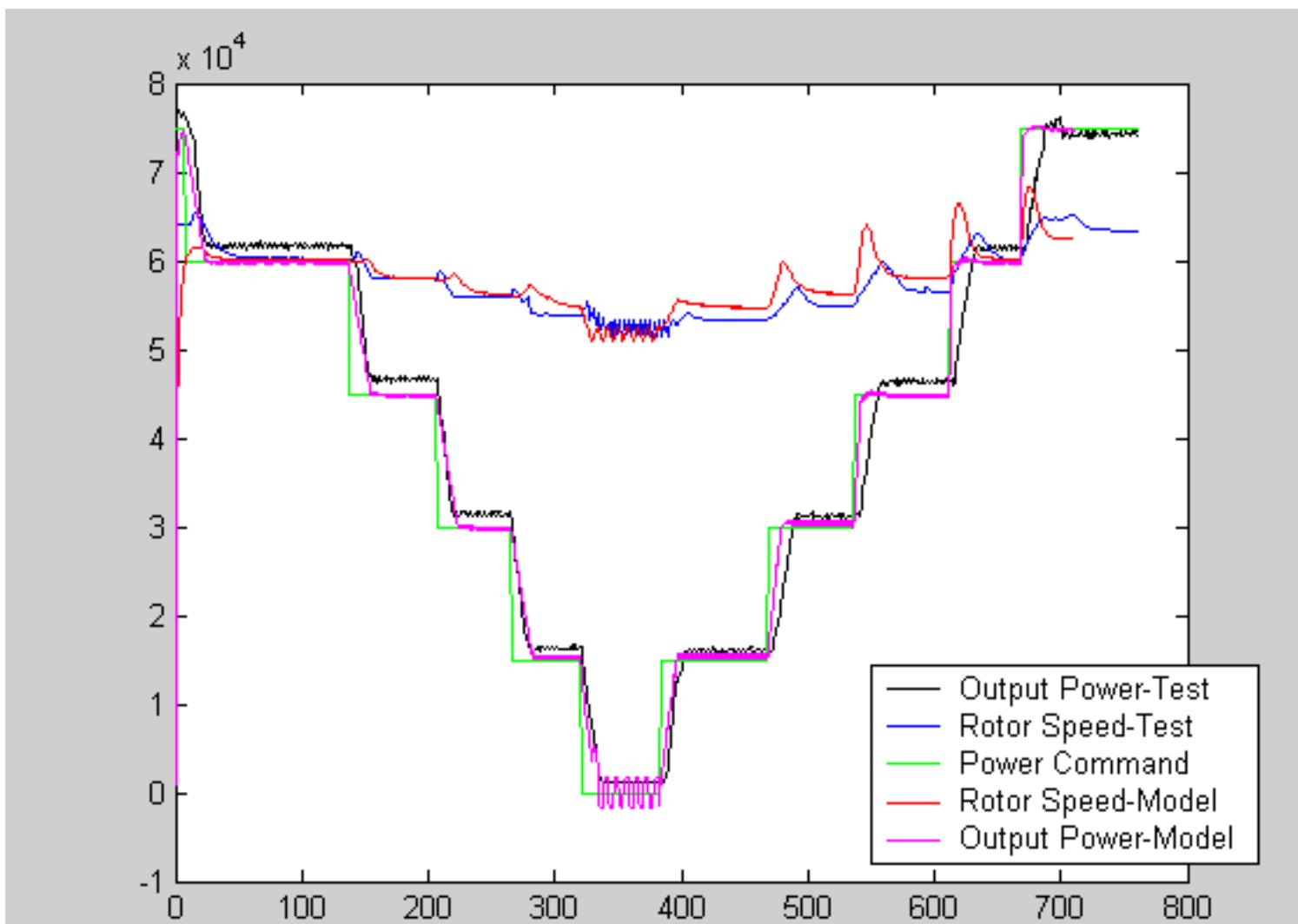
1. PSE



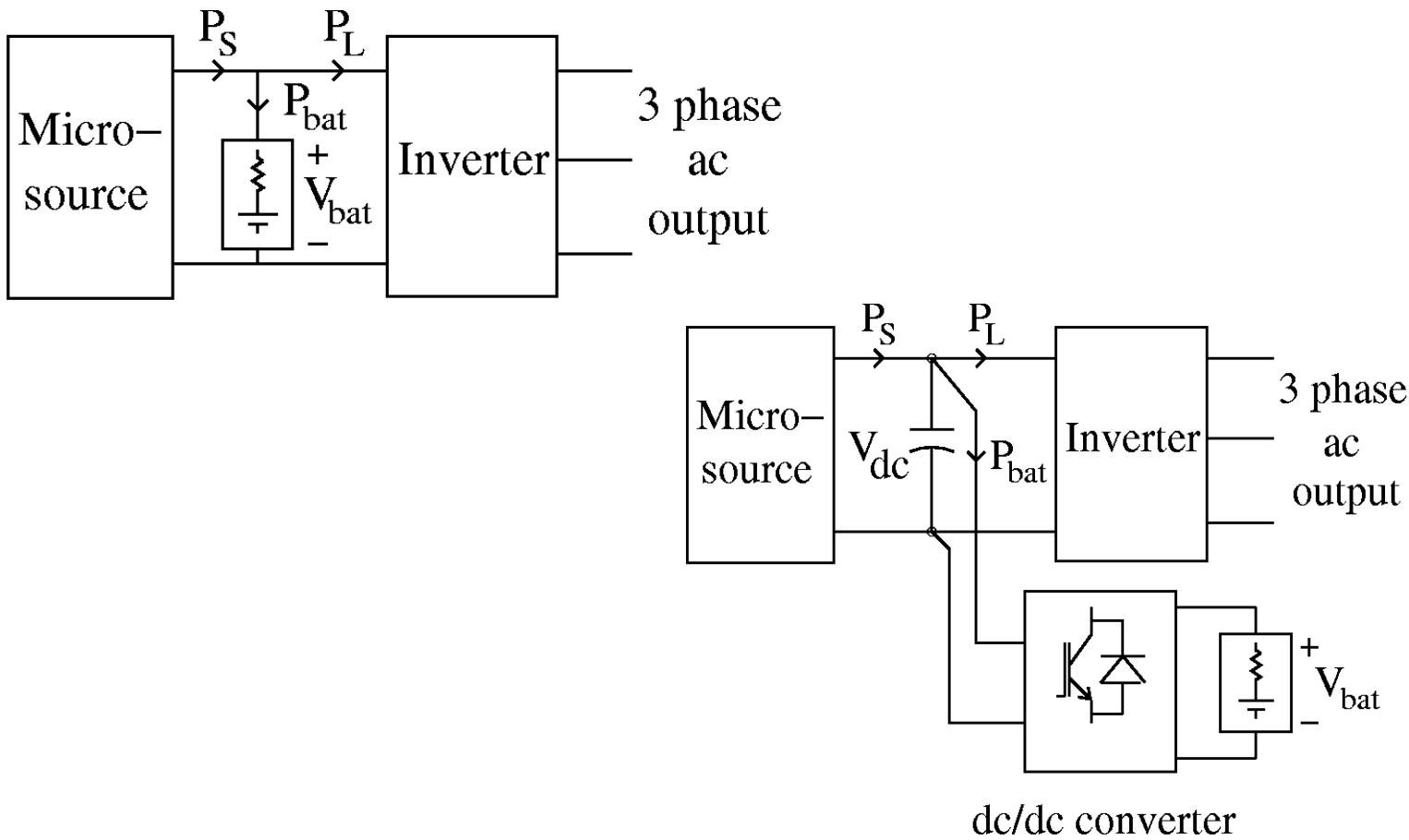
1. PSE



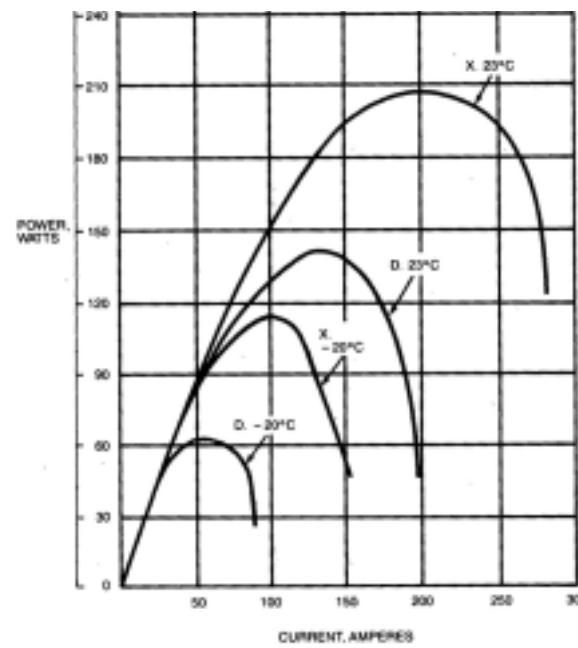
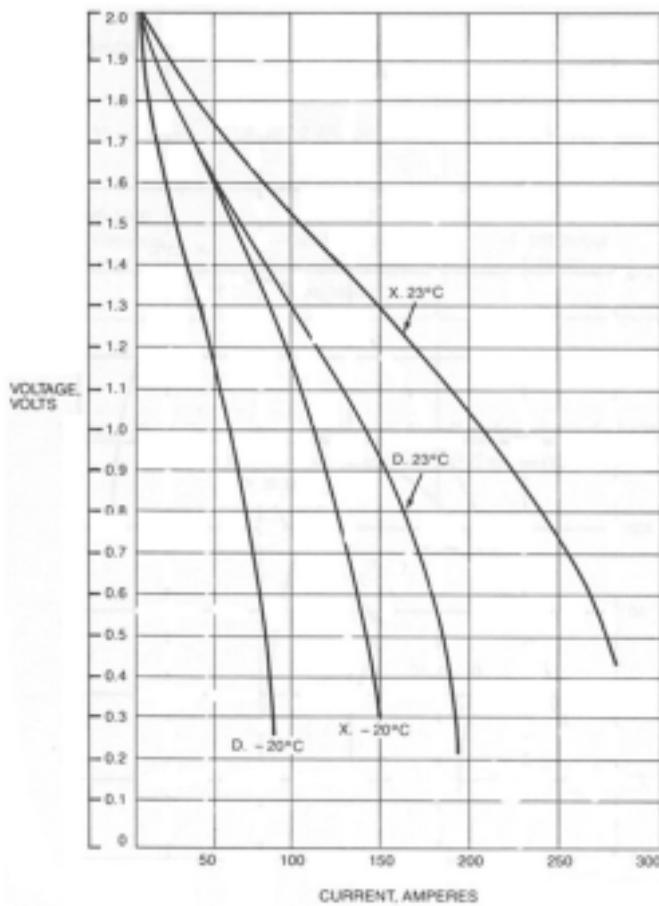
1. PSE



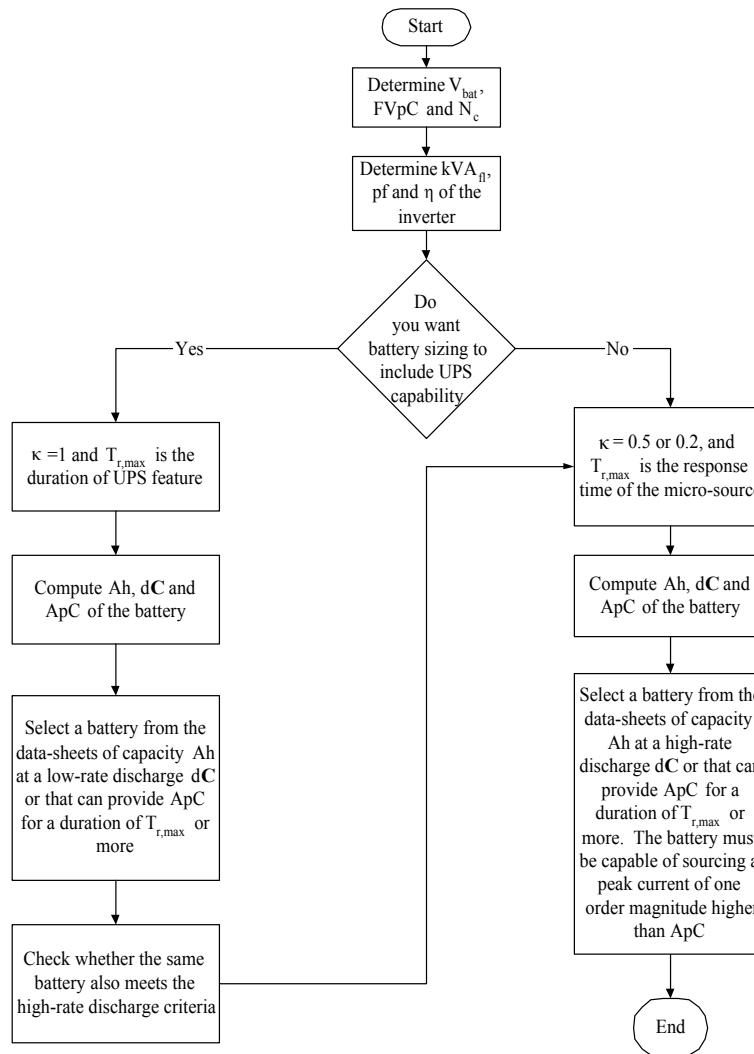
2. ESR



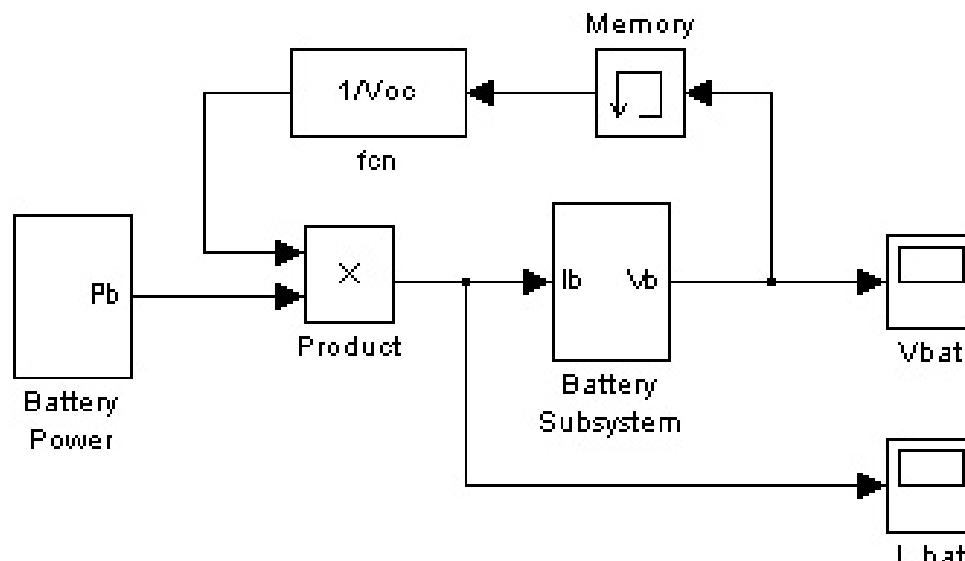
2. ESR



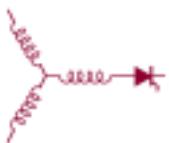
2. ESR



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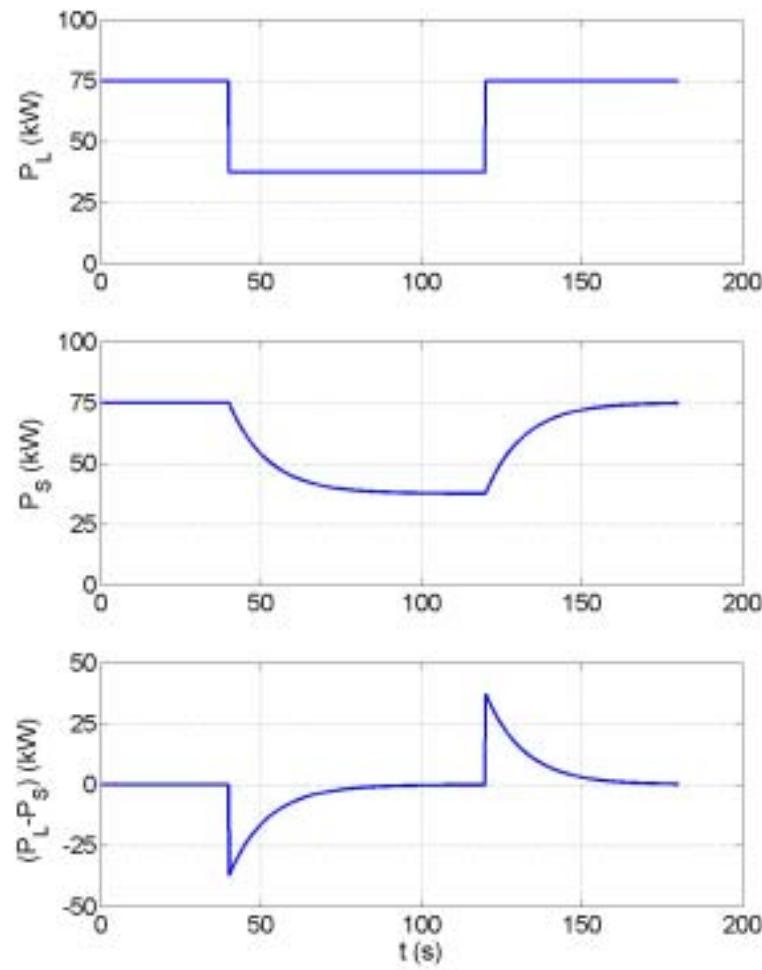


Simulation for Battery Sizing

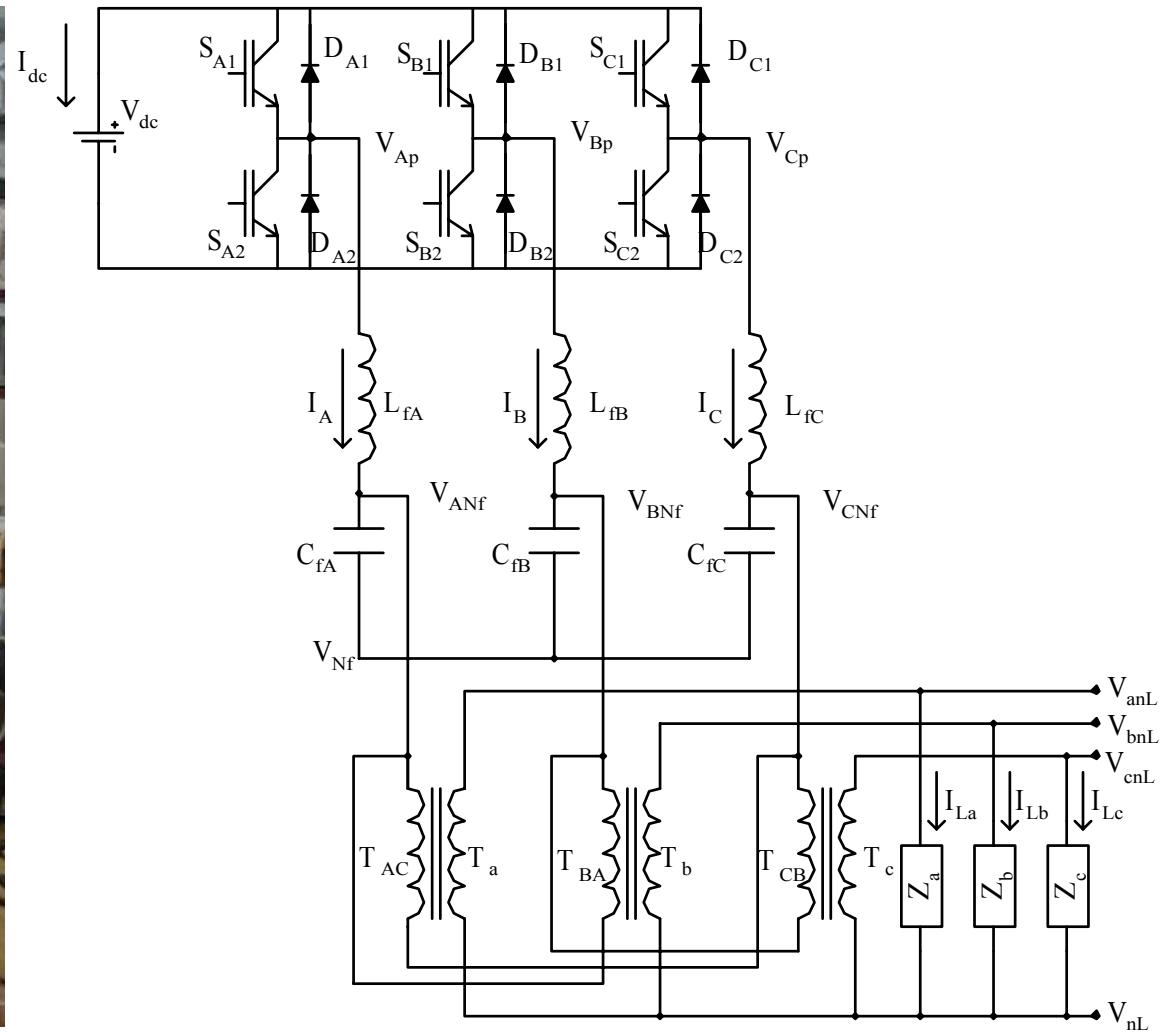


2. ESR

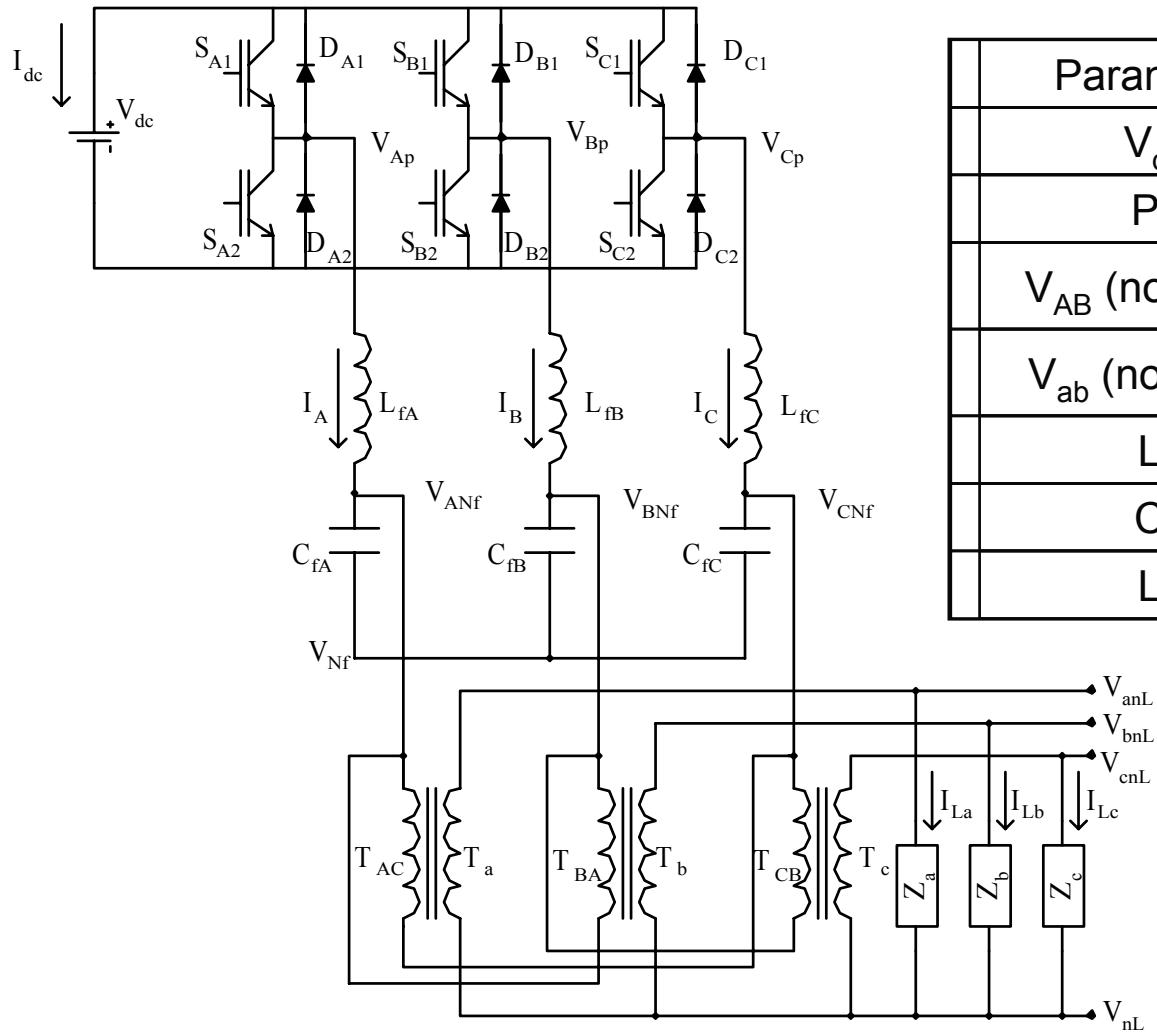
- Fit of sample data of time of response of turbine
- Actual turbine output response time versus step magnitude
- Ramp response



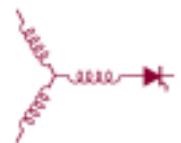
3. DSI



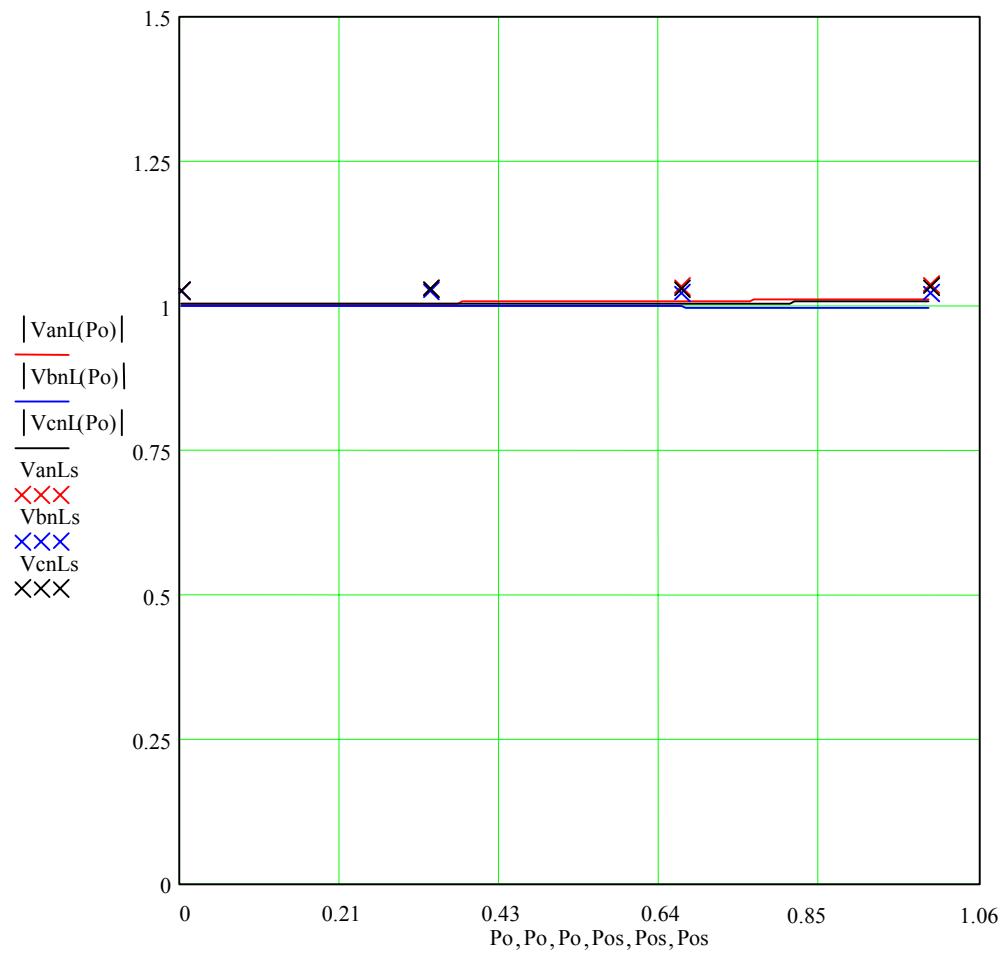
3. DSI



Parameter	Value
V_{dc}	750 V
P_o	15 kW
V_{AB} (nominal)	480 V
V_{ab} (nominal)	208 V
L_f	0.97 mH
C_f	180 μ F
L_t	2.1 mH



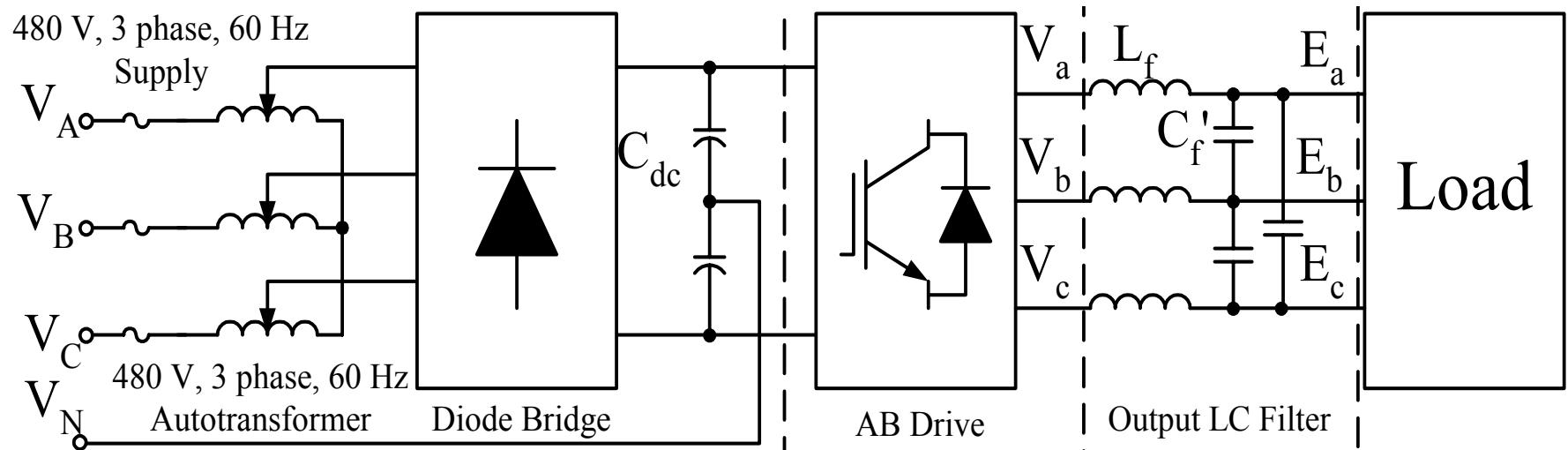
3. DSI



3. DSI

Load		% Regulation		
Type	p.f.	Phase 'a'	Phase 'b'	Phase 'c'
Balanced	1.0	1.5	1.5	1.5
	.45(lag)	1.9	1.9	1.9
	.89(lead)	-0.5	-0.5	-0.5
Unbalanced	1.0	0.89	1.4	0.13
	.45 (lag)	1.7	1.0	0.47
	.89 (lead)	-0.92	0.57	-0.43

3. DSI



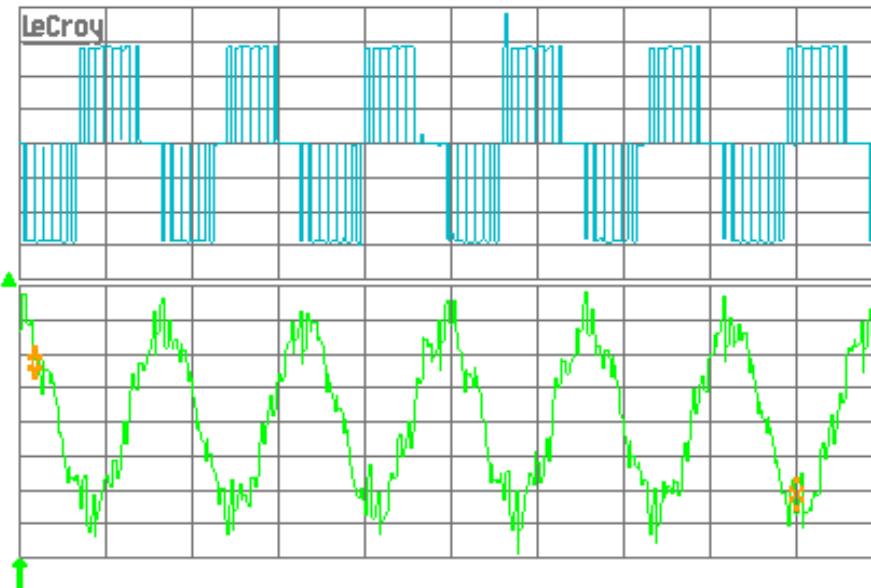
3. DSI

20-Jun-01
17:09:38

Reading Floppy Disk Drive

3
10 ms
250 V

4
10 ms
10.0 A



CHANNEL 3

Trace
OFF On

Coupling

ZOOM

FIND

Gain
Fixed
variable

Offsets in
Volts
 Divisions

Grids
Single Dual
Quad Octal

	11 sweeps:	average	low	high	sigma
pkpk(4)		7.6 A	0.6	76.9	23.0
mean(4)		-0.23 A	-0.64	-0.18	0.14
sdev(4)		1.90 A	0.16	19.29	5.77
rms(4)		1.98 A	0.25	19.28	5.74
10 ms BWL ampl(4)		4.2 A	0.6	38.8	11.5

1 .1 V DC $\frac{500}{\text{mV}}$

2 10 mV 500 $\frac{\text{mV}}{\text{mV}}$

3 .5 V DC $\frac{500}{\text{mV}}$

4 .5 V AC $\frac{20}{\text{mV}}$

5 kS/s

STOPPED

4 HFREJ 40.0 A

3. DSI

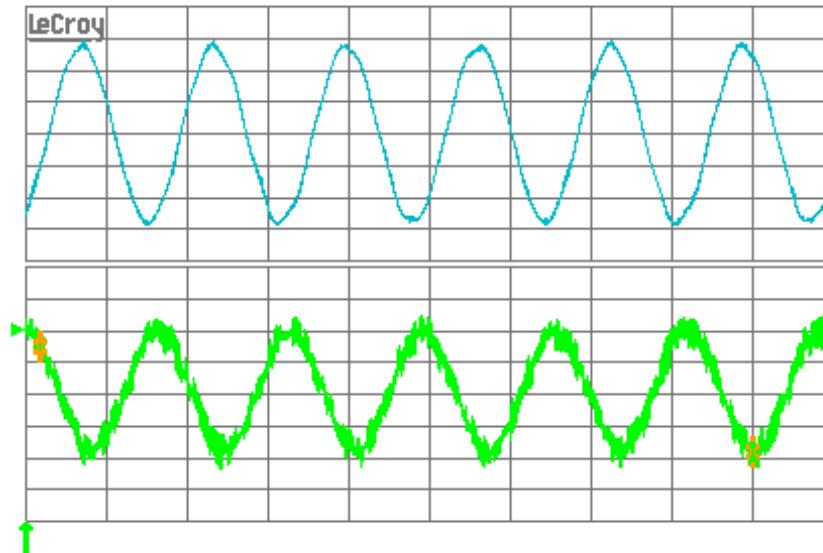
20-Jun-01
17:00:19

Not Enough Space on Device (Full)

3
10 ms
250 V

LeCroy

4
10 ms
2.00 A



TIMEBASE
T/div 5 ms
500 samples at
10 kS/s
(100 μ s/pt)
For 50 ms

Sampling
Single Shot

Sample Clock
Internal
ECL 0V TTL

Sequence
OFF On
Record up to
500 samples

	1 sweeps:	average	low	high	sigma
pkpk(4)		9.63 A	9.63	9.63	- - -
mean(4)		-200 mA	-200	-200	- - -
sdev(4)		2.601 A	2.601	2.601	- - -
rms(4)		2.608 A	2.608	2.608	- - -
5 ms BWL ampl(4)		6.96 A	6.96	6.96	- - -

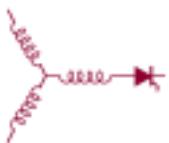
1 .1 V DC $\frac{1}{500}$
2 10 mV 50Ω $\frac{1}{500}$
3 .5 V DC $\frac{1}{500}$
4 .1 V AC $\frac{1}{20}$



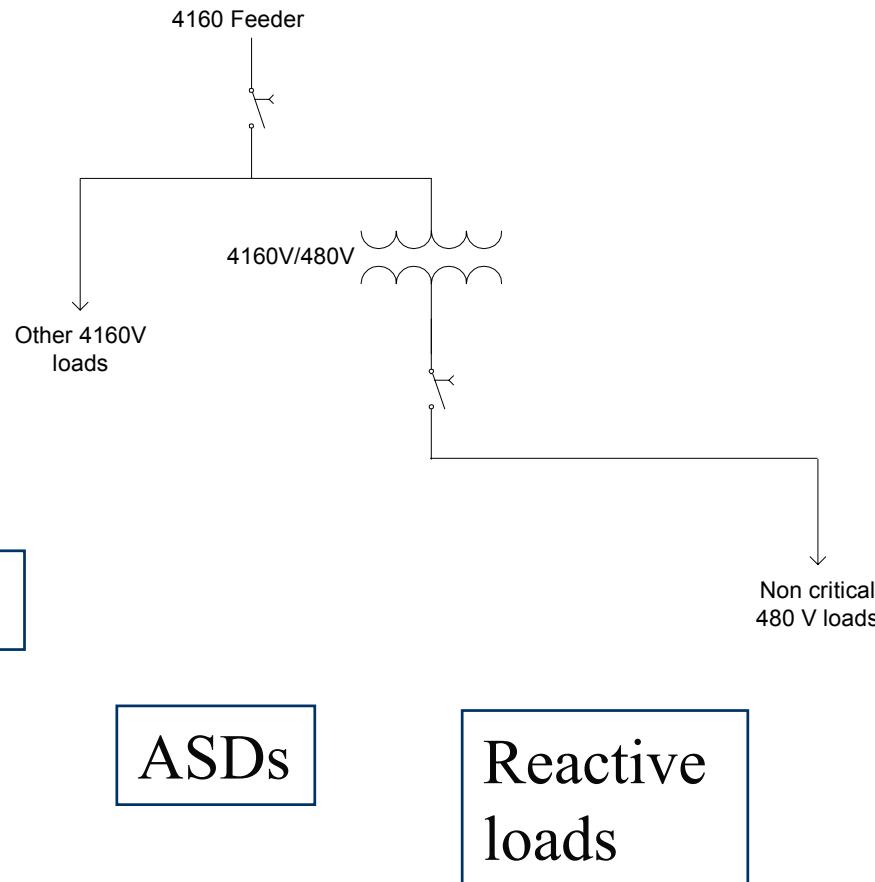
4 HFRDJ 3.80 A

10 kS/s

STOPPED



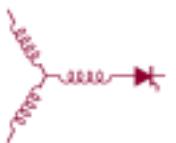
3. DSI



3. DSI



- Cable tray system for interconnections installed
- Physical plant wiring modifications completed
- Being extended to add additional loads
- Load center with measurement interface being incorporated



4. DGC

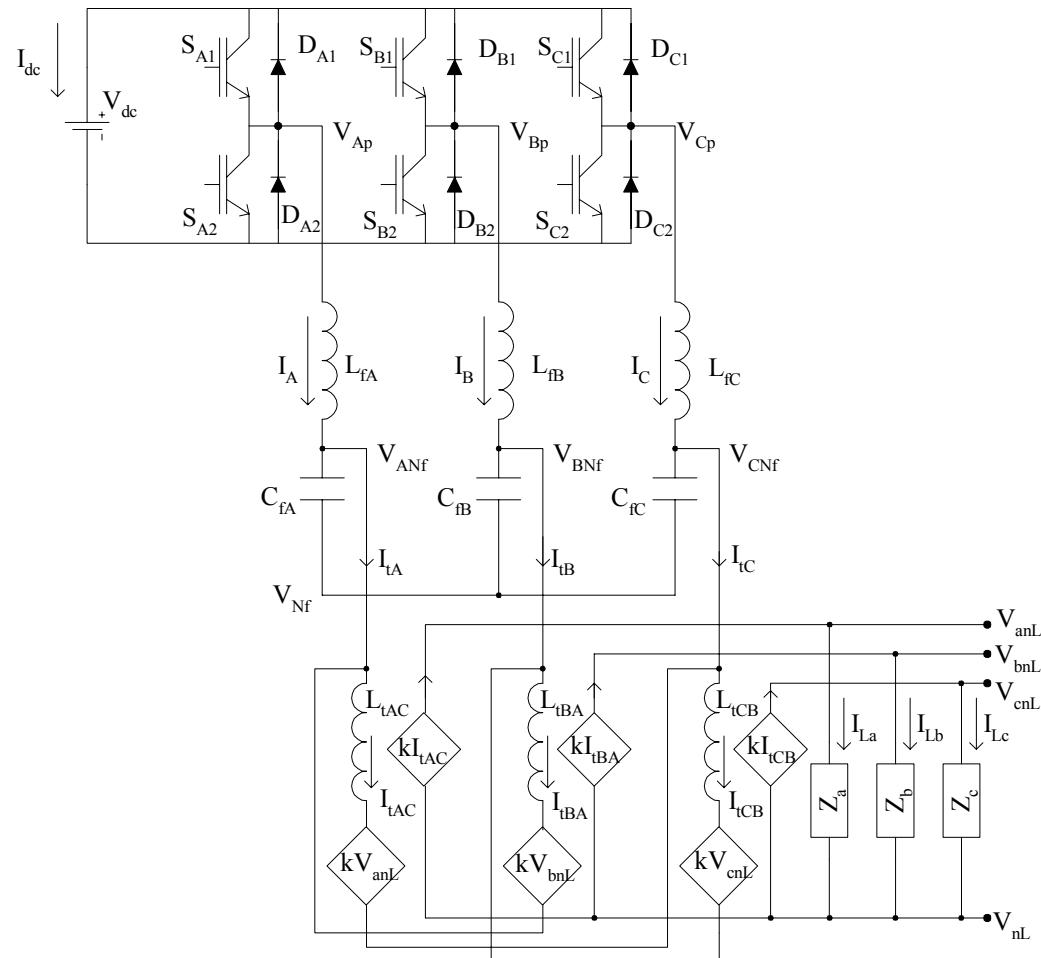
- CTs, PTs analog interface completed
- Software platform completed
- DSP control output interface being developed

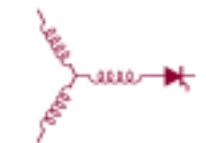


5. CSS

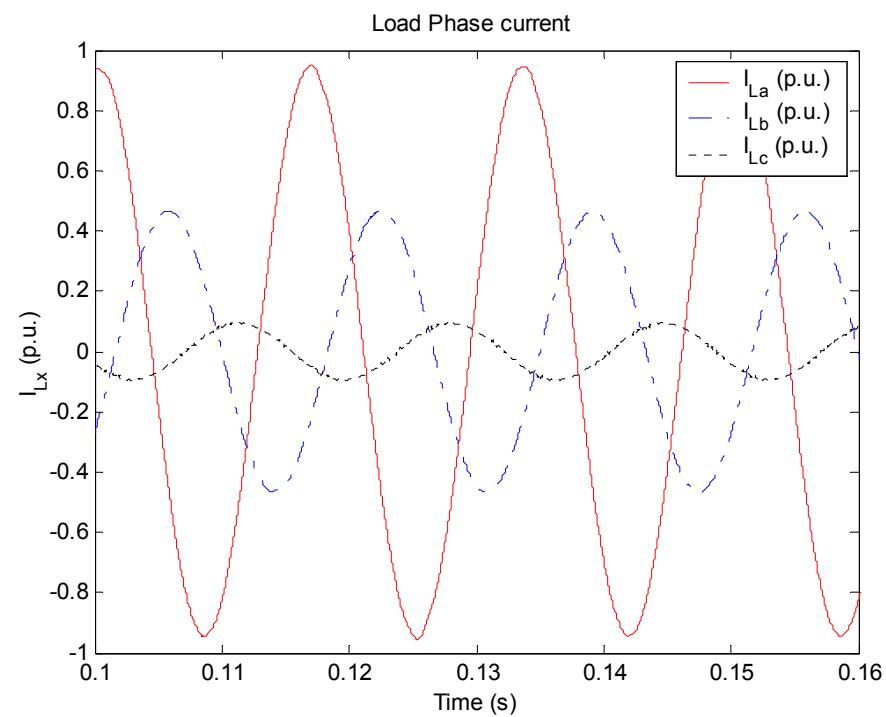
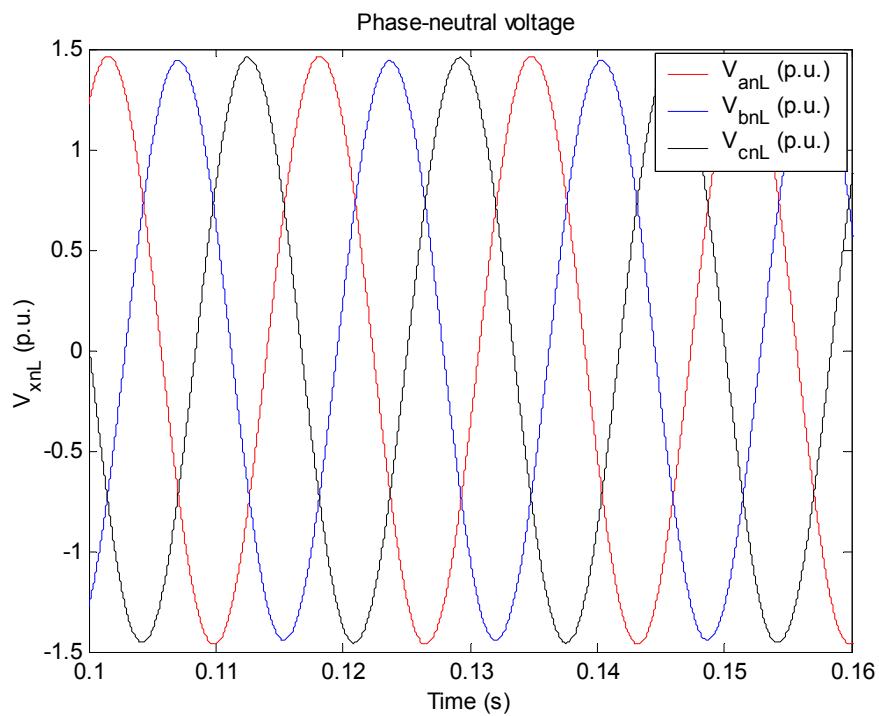
- Several computer simulation models in process
 - EMTP
 - Saber
 - Matlab-Simulink
 - Matlab
 - Mathcad

5. CSS

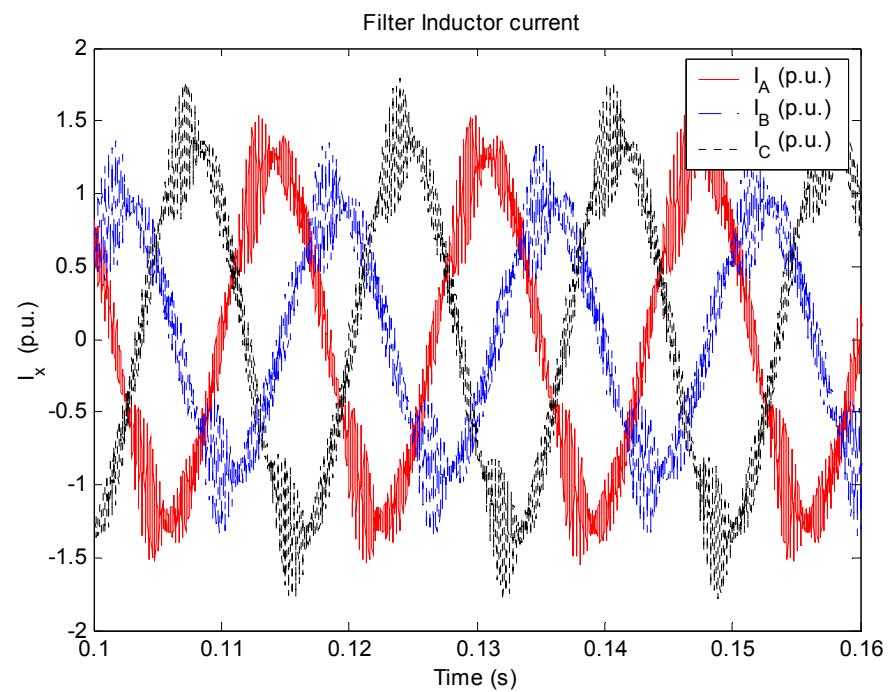
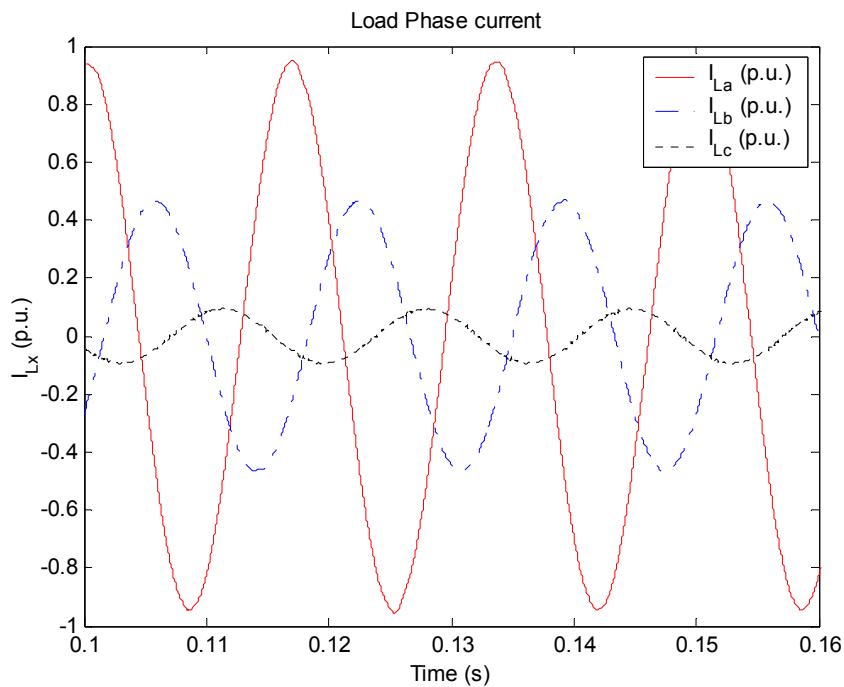




5. CSS



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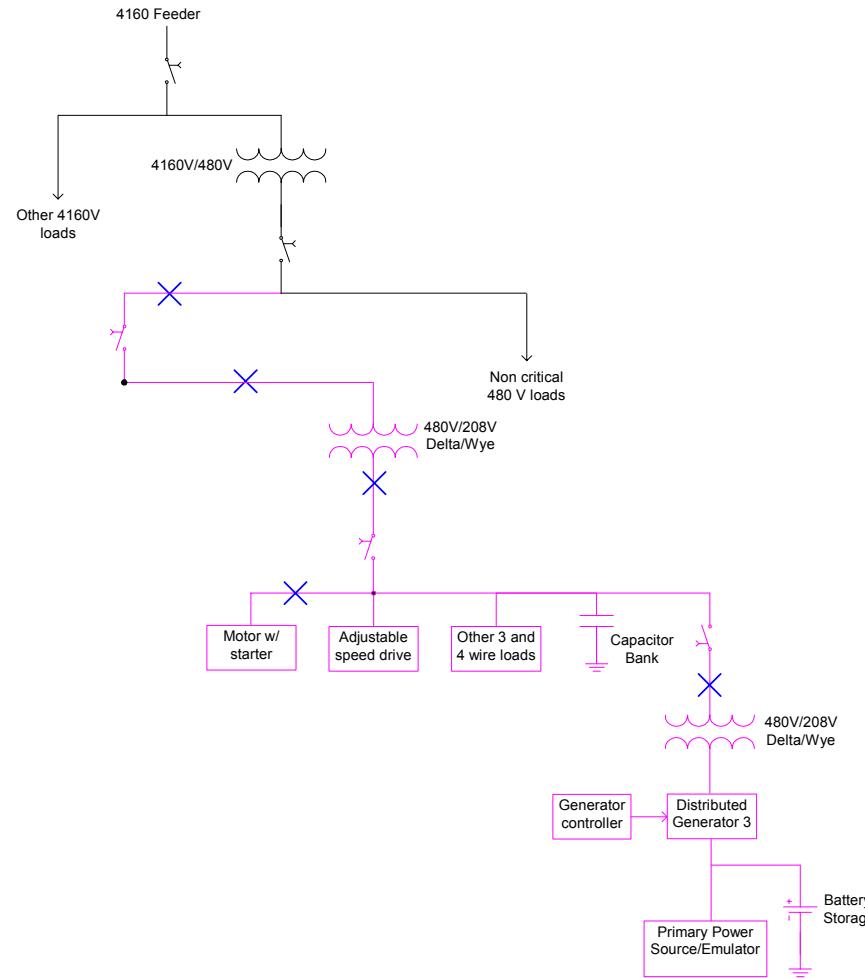


Year 1 Tasks

ID	Task Name	Start Date	End Date	Duration	2000			2001				2002	
					Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
1	Development of power source emulator	12/15/00	12/3/01	252d					██████████	██████████	██████████		
2	Study of energy storage requirements	12/16/00	3/30/01	75d				████	██████████				
3	Demonstration of single inverter feeding complex loads	12/20/00	12/5/01	251d				██████████	██████████	██████████	██████████		
4	Development of DG inverter control	12/20/00	7/11/01	146d			████	██████████	██████████				
5	Computer simulation for Tasks 1-5	12/17/00	12/10/01	256d				██████████	██████████	██████████	██████████		
6	Expansion of lab scale microgrid												
7	Development of second PSE and Inverter												
8	Demonstration of two islanding and reconnection												
9	Demonstration of power quality solutions												
10	Computer simulation for Tasks 6-9												
11	Expansion fo lab scale microgrid												
12	Development of third PSE and Inverter												
13	Demonstration of decentralized control												
14	Demonstration of power quality solutions												
15	Demonstration of operation under faults												
16	Computer simulation for Tasks 11-15												

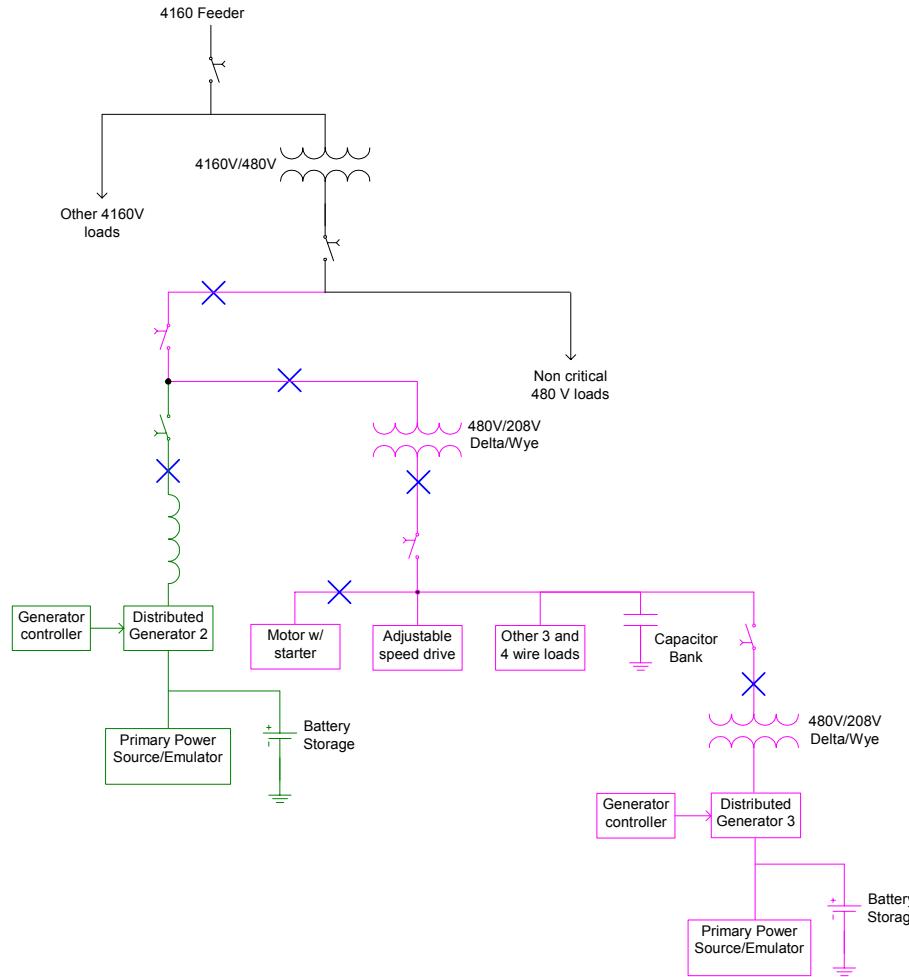
Evolution of Platform (Year 1)

- Single inverter
- Complex set of loads



Evolution of Platform (Year 2)

- Two inverters
- Islanding and reconnection
- Correcting power quality events (balanced)



Evolution of Platform (Year 3)

- Three inverters
- Decentralized control
- Single phase power quality events
- Fault management

